

Figure 1

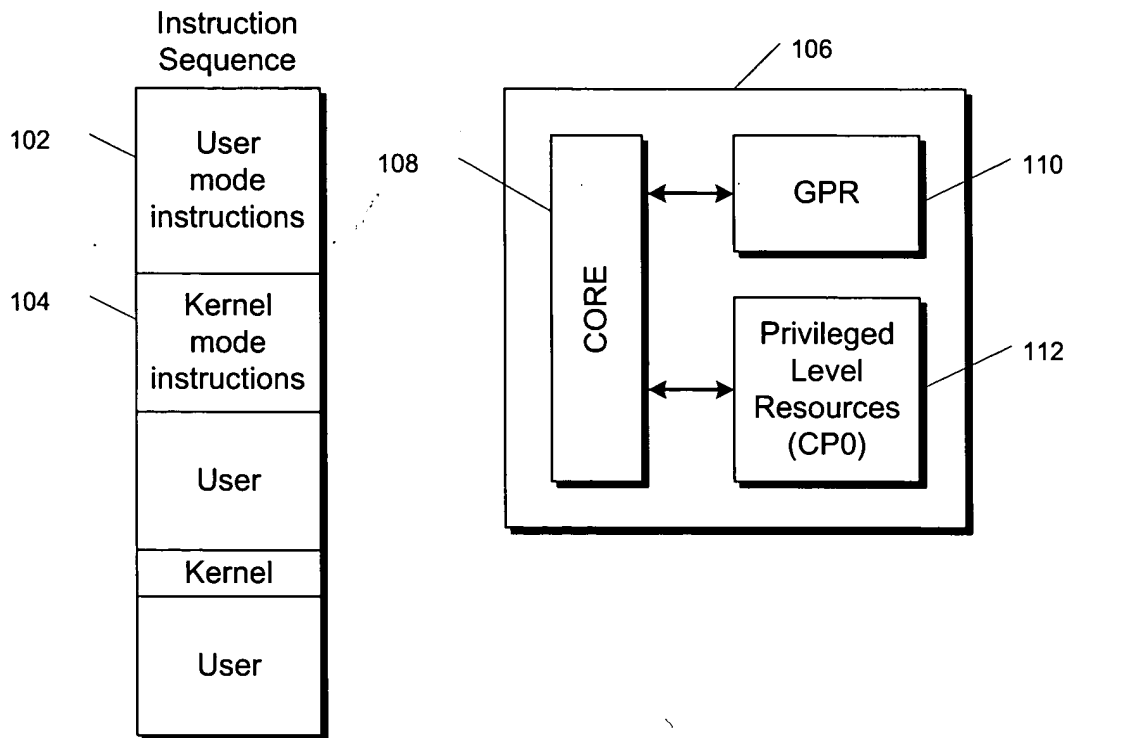


Figure 2

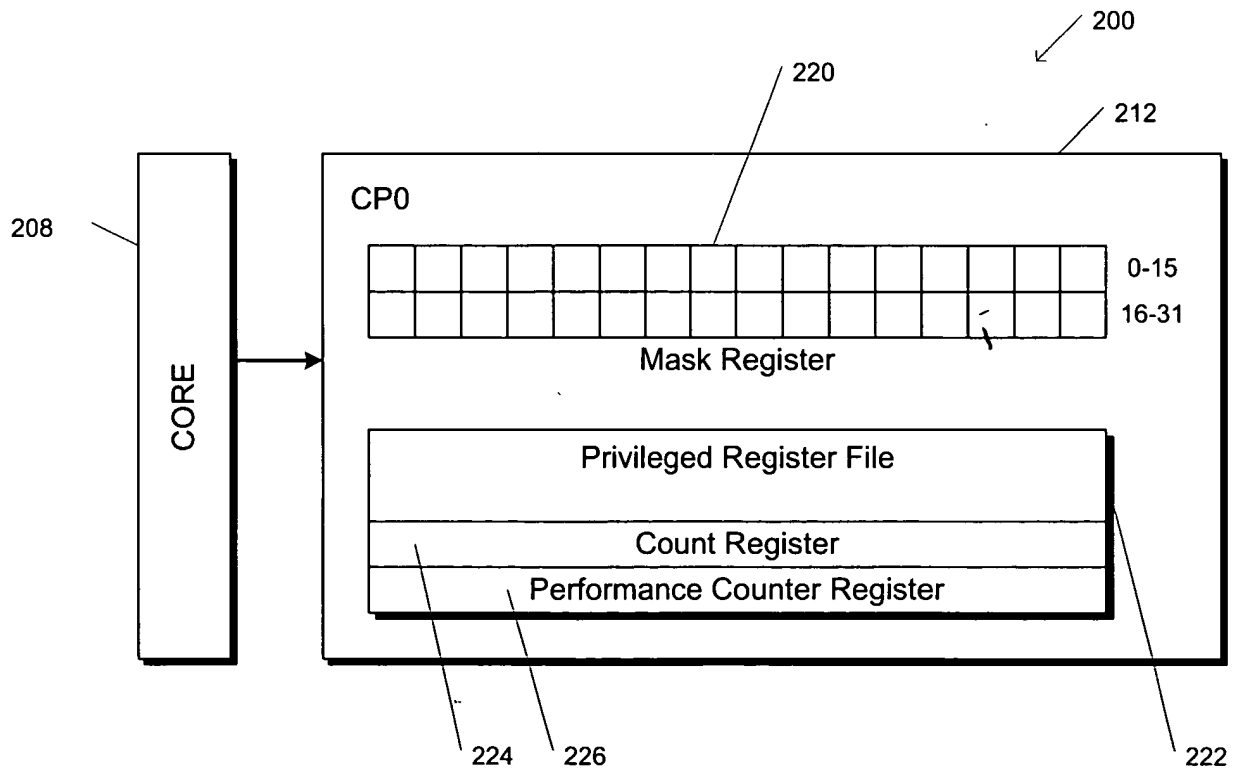


Figure 3

Flow Chart for update of Read-only Mask Register

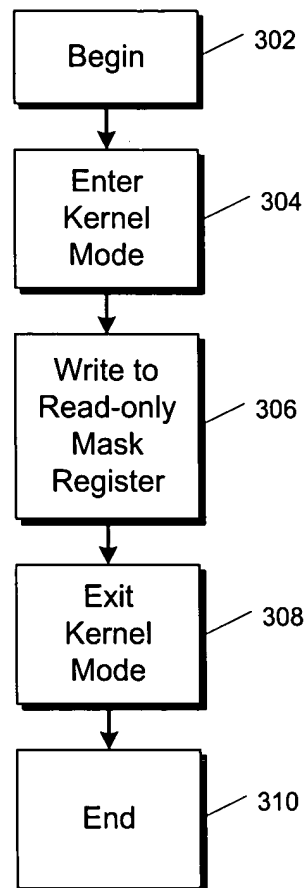


Figure 4

Write to CP0 Register

400

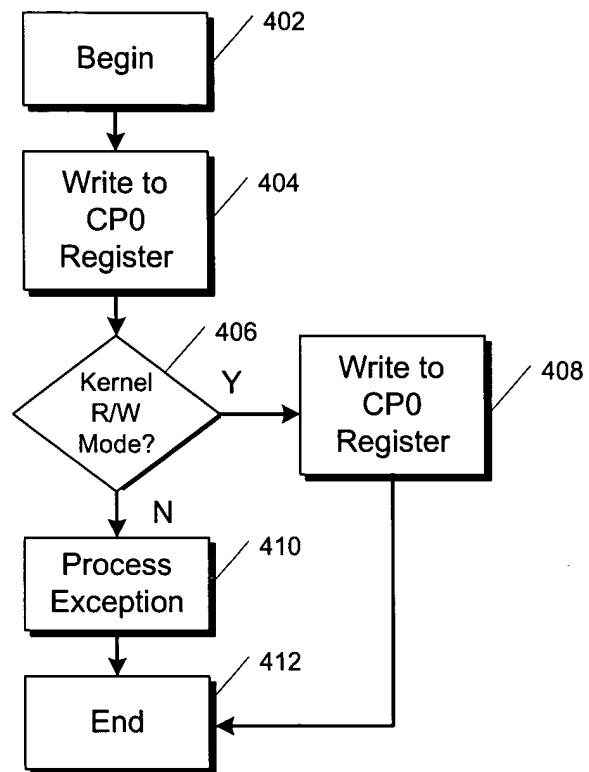


Figure 5

Read from CP0 Register

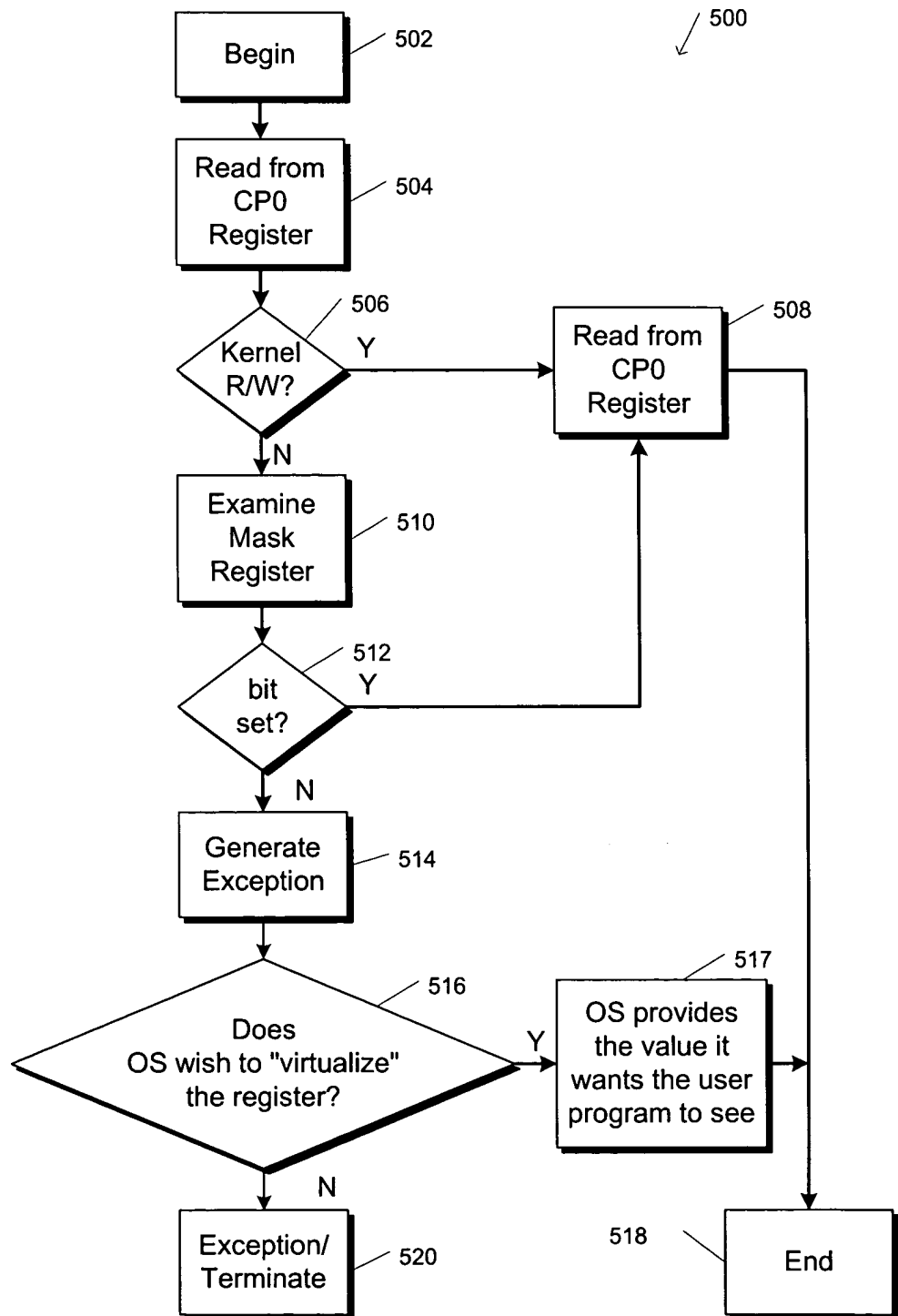


Figure 6

600
↙

Mnemonic	Function
RDC0	Move from Coprocessor Zero (Read-only)
DRDC0	Doubleword Move from CP0 (Read-only)
MTC0	Move to CPO bit mask (Kernel Mode only)